Claim Listing

Claims 1-28 are now cancelled without prejudice.

29. (New) A system for displaying images, said systems comprising:

a first processor for decoding the images in a decoding order; and

a second processor for determining a display order for the images, wherein the display order is different from the decoding order; and

wherein the first processor prepares the decoded images for display in the display order determined by the second processor.

30. (New) The system of claim 29, wherein the first processor provides parameters associated with the images, and wherein the second processor determines the display order based on the parameters associated with the images that are provided by the first processor.

31. (New) The system of claim 29, further comprising a first memory for storing a first plurality of instructions that are executed by the first processor and a second memory for storing a second plurality of instructions that are executed by the second processor.

32. (New) The system of claim 31, wherein the second memory stores parameters provided by the second processor, and wherein the second processor determines the display order based on the parameters stored in the second memory.

33. (New) The system of claim 31, wherein the second memory stores the decoded images.

34. (New) The system of claim 31, wherein the first memory comprises an SRAM, and wherein the second memory comprises a DRAM.

35. (New) The system of claim 29, wherein between a vertical synchronization signal and a next vertical synchronization signal, the first processor decodes a particular one of the images, and wherein the second processor selects a display image for display following the next vertical synchronization signal.

36. (New) The system of claim 35, wherein the first processor provides parameters associated with the particular one of the images, and wherein the second processor selects the display image based on the parameters associated with the particular one of the images.

37. (New) The system of claim 35, wherein the second processor notifies the first processor of the display images, and wherein the first processor prepares the display image for display following the next vertical synchronization signal.

38. (New) The system of claim 29, wherein the images are selected from a group consisting of pictures, frames, top fields, and bottom fields.

39. (New) A circuit for displaying images, said circuit comprising:

a processor; and

a memory connected to the processor, said memory storing a plurality of instructions that are executable by the processor, wherein execution of the instructions by the processor causes:

decoding the images in a decoding order;

receiving an indication from another processor, said indication indicating a display image in a display order, wherein the display order is different from the decoding order; and

preparing the display image for display.

40. (New) The circuit of claim 39, wherein execution of the instructions also causes:

writing the decoded images to another memory.

41. (New) The circuit of claim 39, wherein execution of the instructions also causes:

writing the parameters to the another memory.

42. (New) The circuit of claim 39, wherein decoding the images in the decoding order further comprises decoding, between a vertical synchronization signal and a next vertical synchronization signal, a particular image; wherein receiving the indication, further comprises receiving the indication between the vertical synchronization signal and the next vertical

synchronization signal; and wherein preparing the display image for display comprises preparing the display image for display following the next vertical synchronization signal.